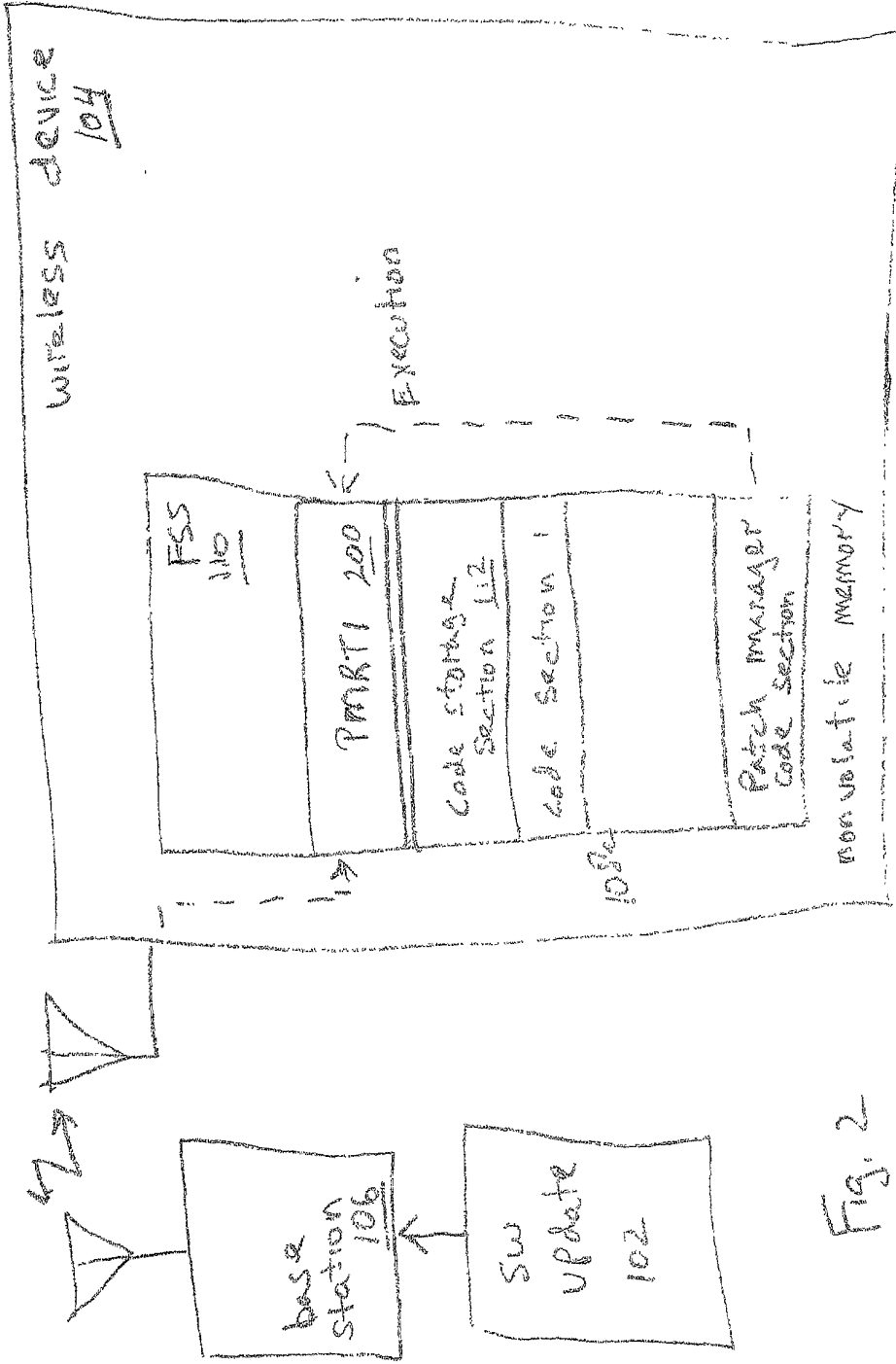


Fig. 1



25

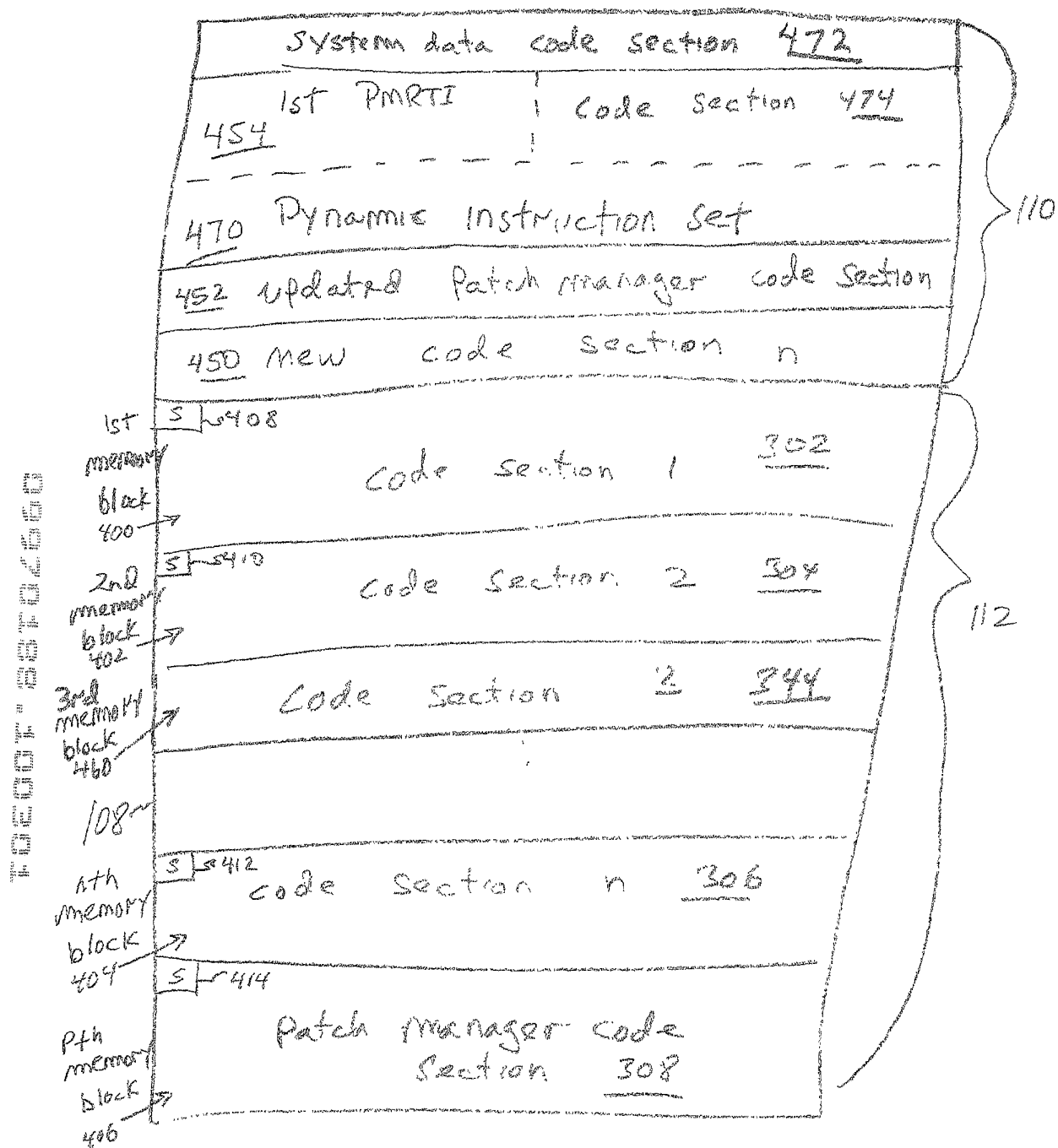


Fig. 4

326

code section address table	
Identifiers	Addresses
CS-1	start address 1 (00100)
CS-2	start address 2 (00200)
⋮	
CS-n	start address n (00700)
PM	start address P (01000)

Fig. 5

FOUO 00402560

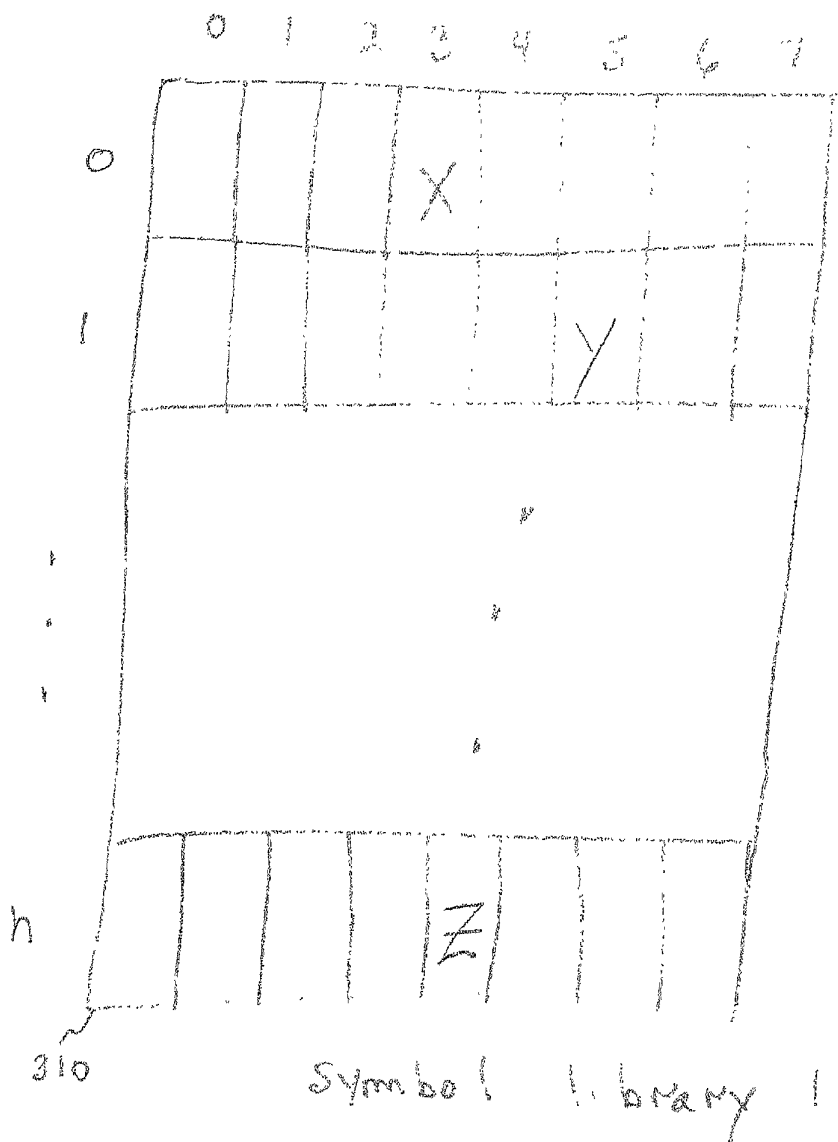


Fig. 6

SECRET 88092600

Symbol offset address table		
Symbol ID	code section ID	Offset
X-1	CS-1	03
Y-1	CS-1	15
P-1	CS-2	11
Q-1	CS-2	33
AA-3	CS-2	47
⋮		

328

Fig. 7

Diagram illustrating the layout of instruction memory:

1st instruction	<u>800</u>
2nd instruction	<u>802</u>
...	...
jth instruction	<u>804</u>

A bracket on the right side of the diagram indicates a range from 470 to 804.



Fig. 8a

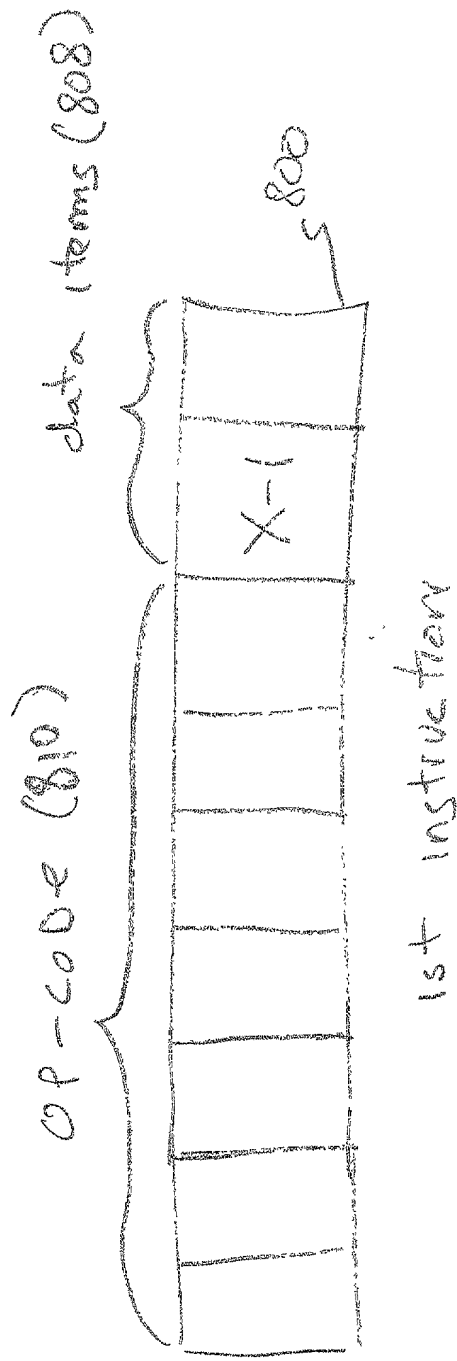


Fig. 8b

FIG. 9

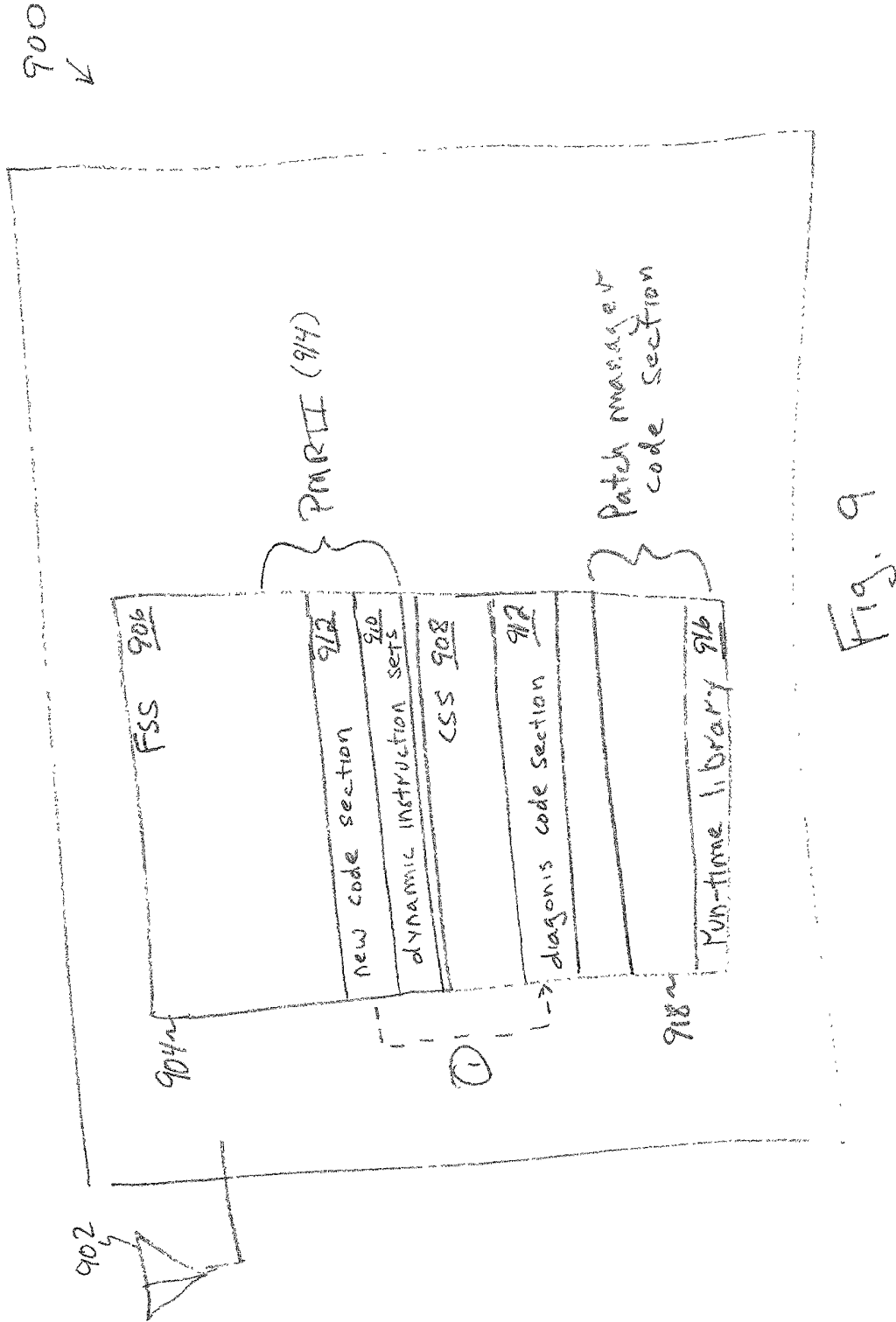


FIG. 10

900
↓

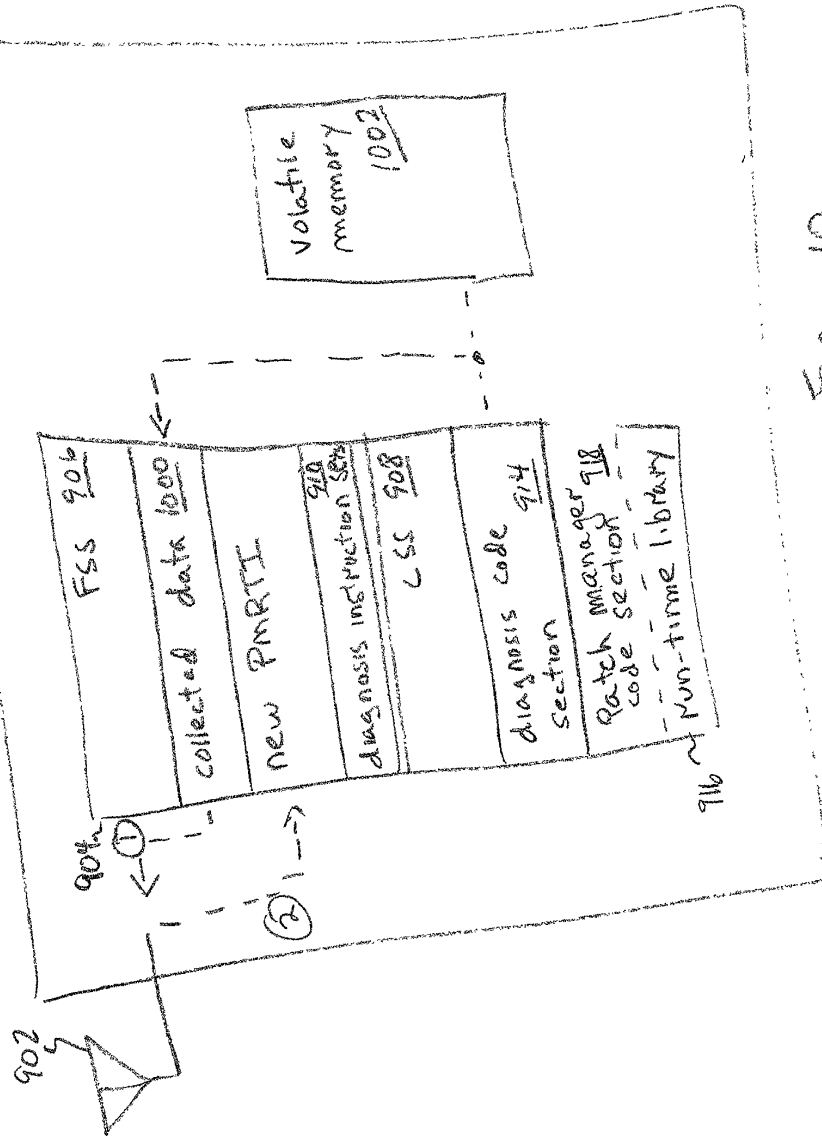
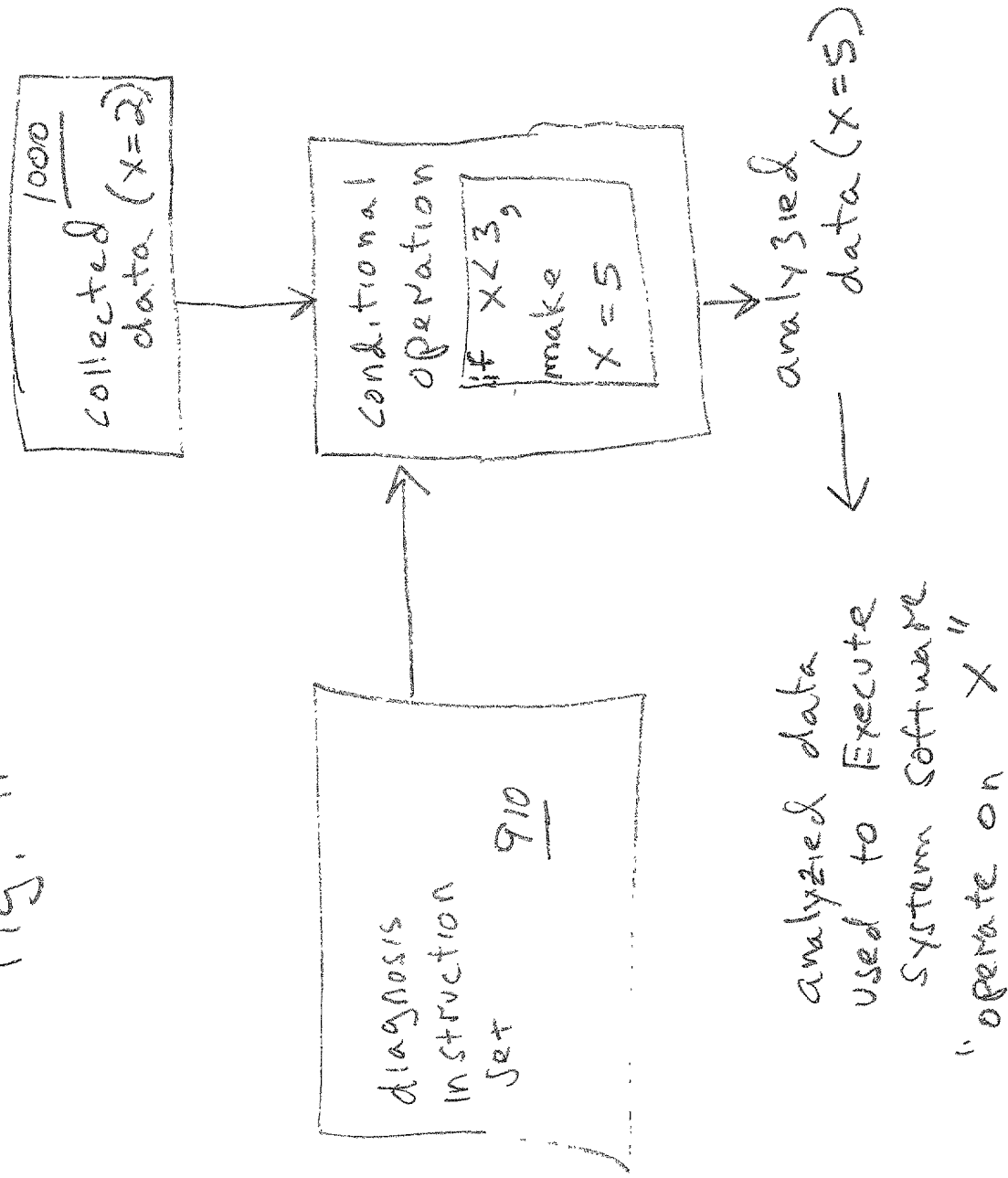
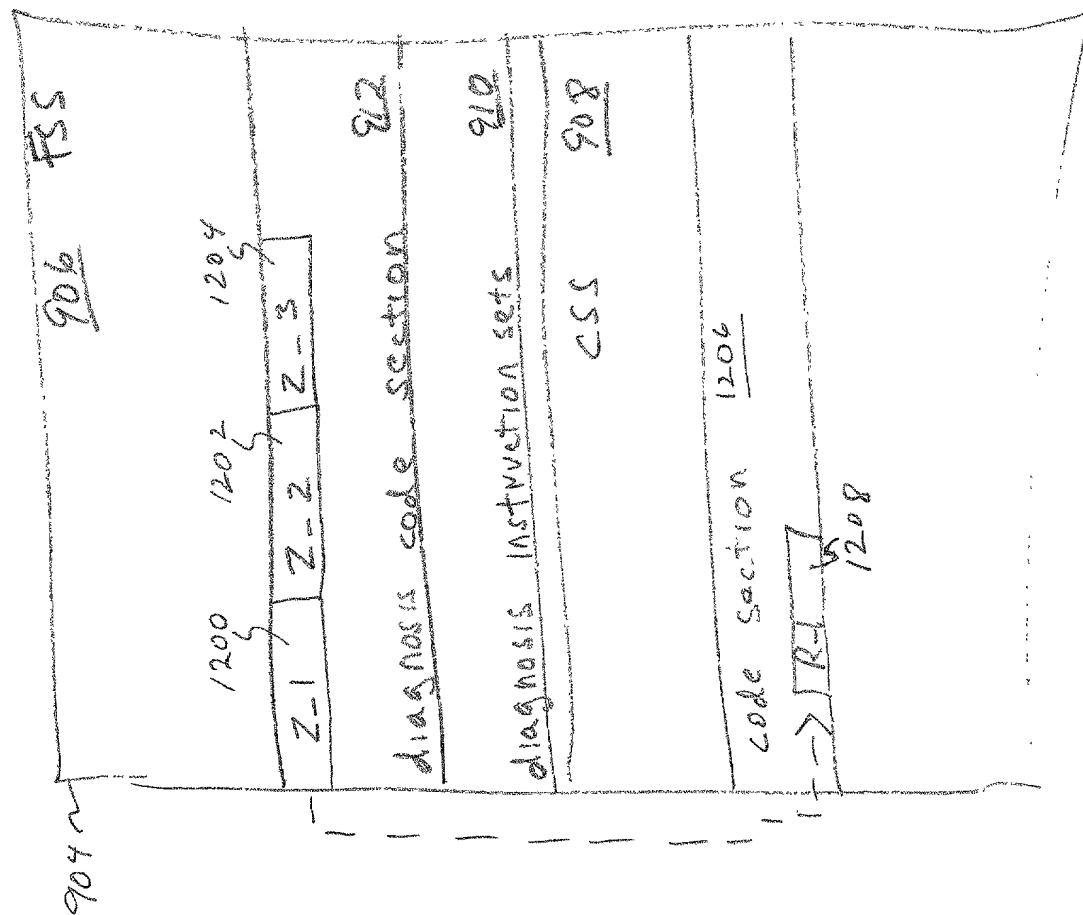


Fig. 10

Fig. 11



003



2
15

REPORT 8870200

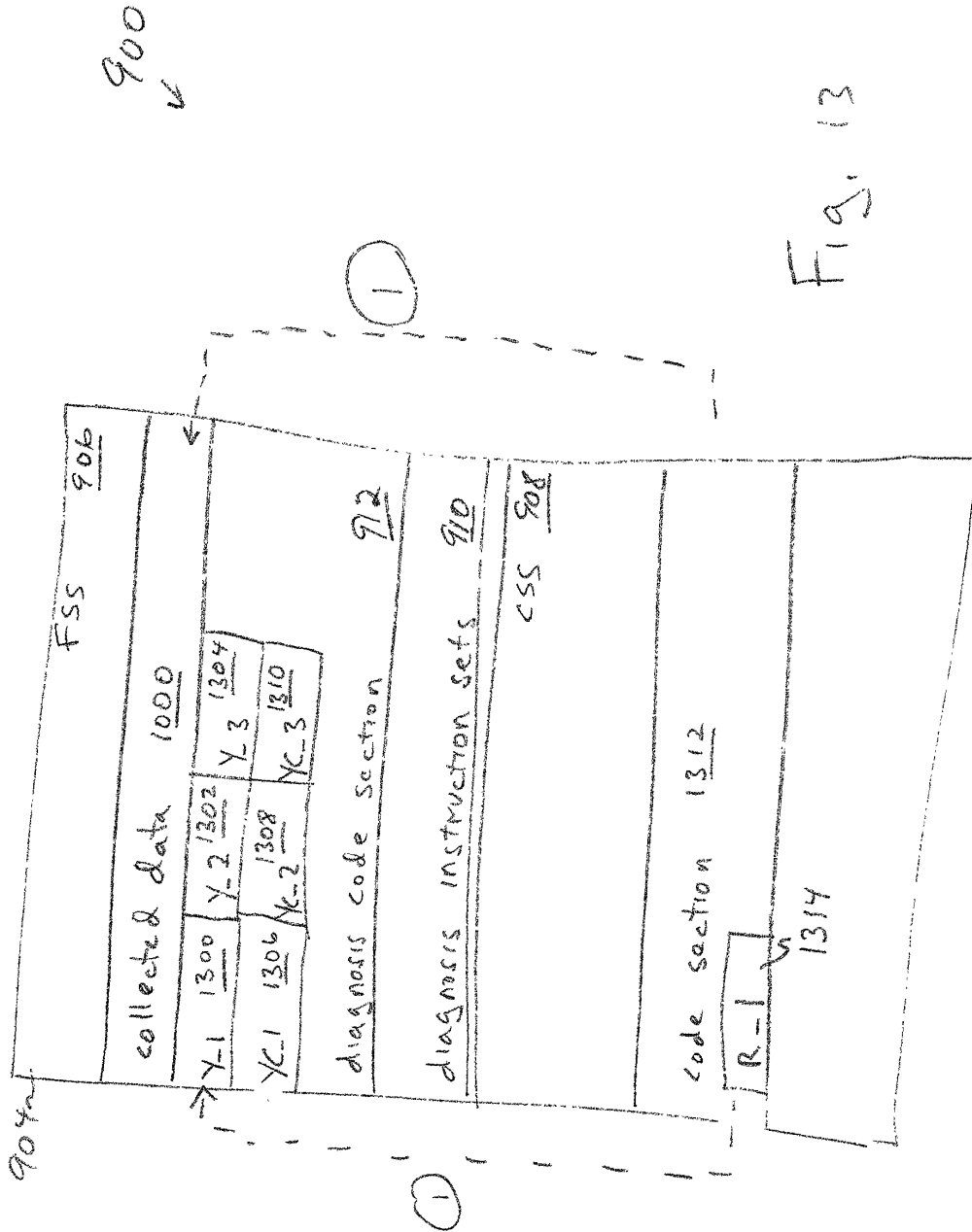


Fig. 13

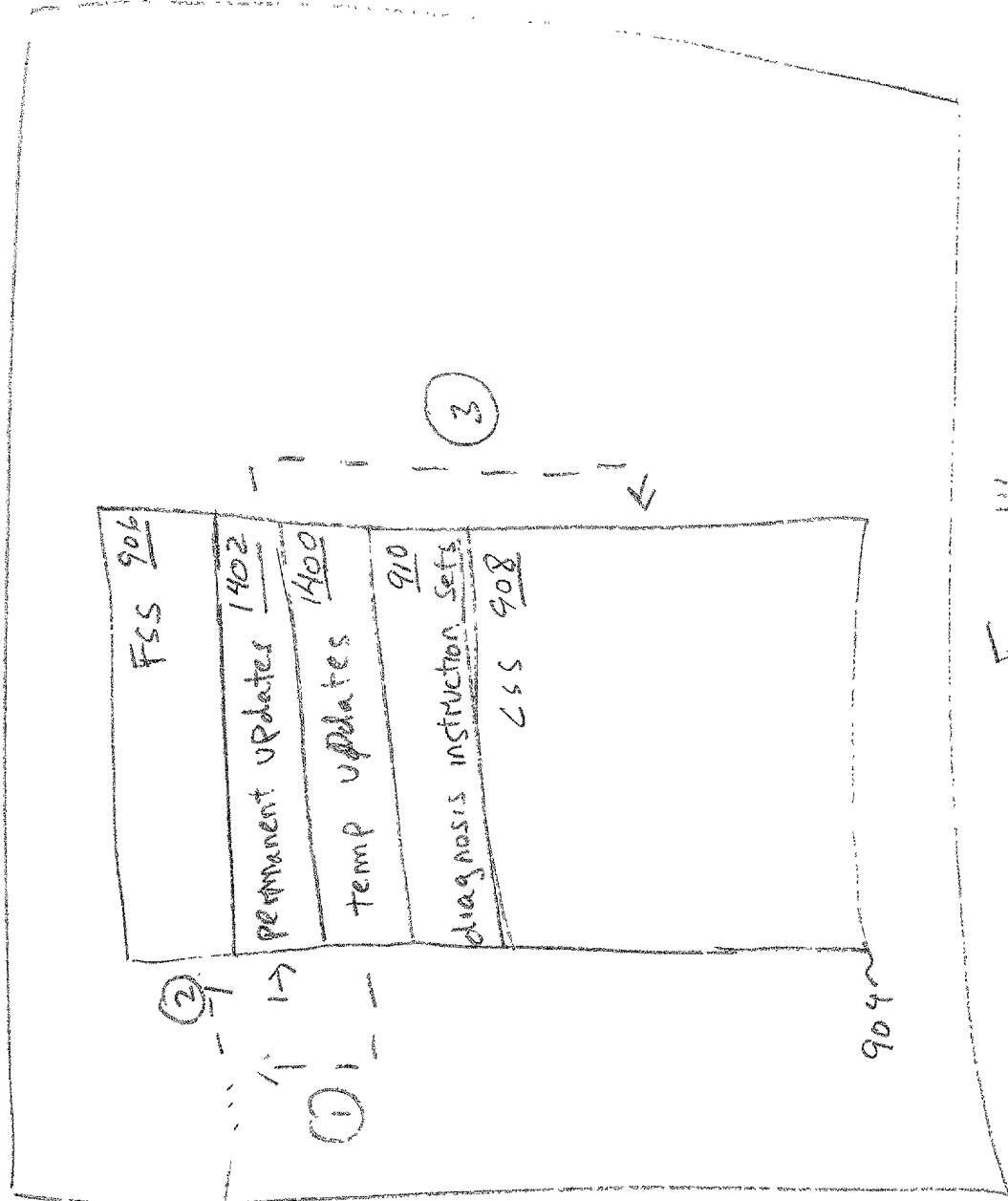
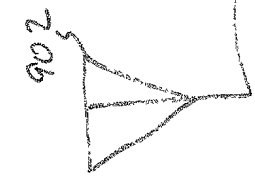


Fig. 14

FIG. 156

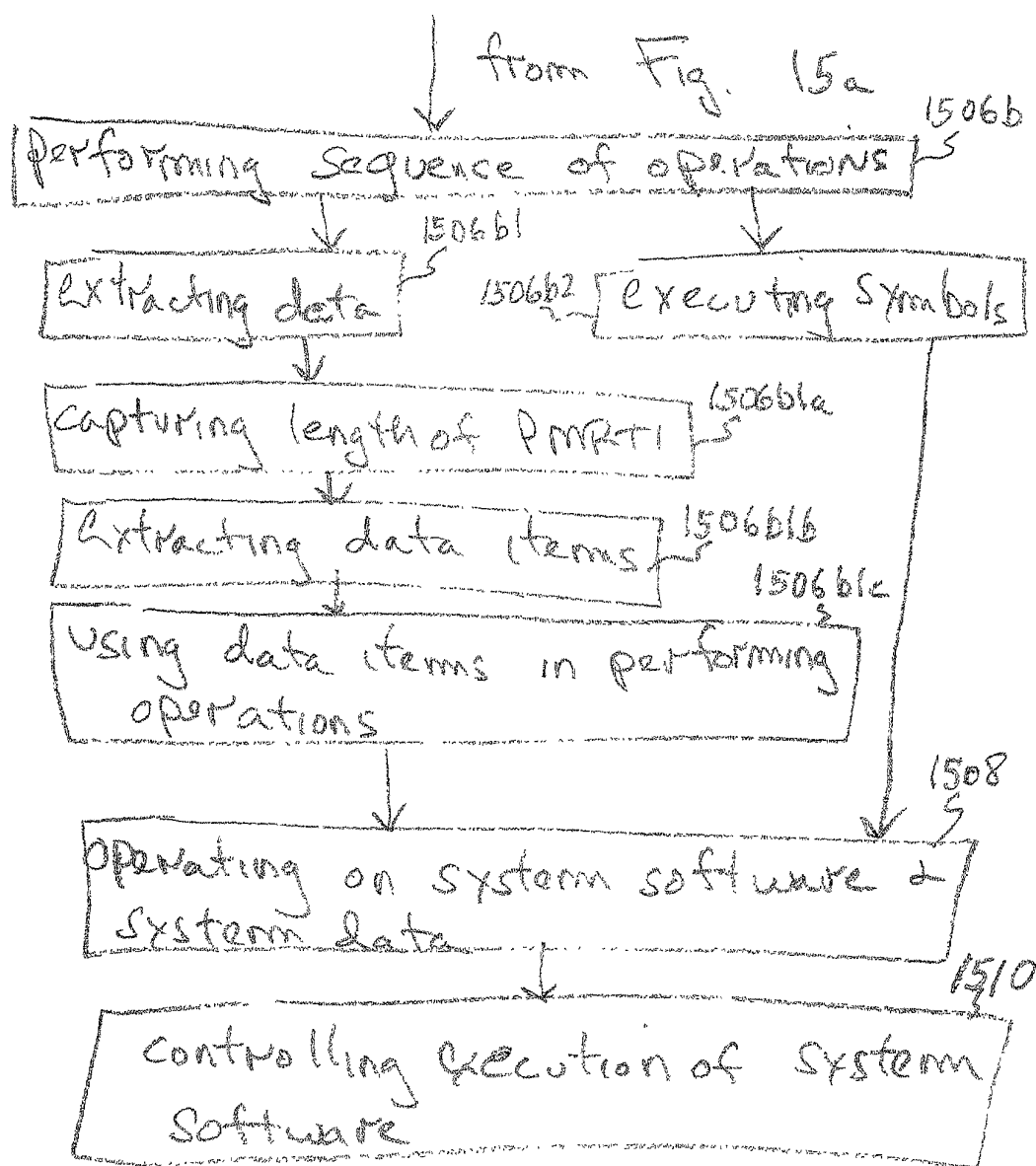
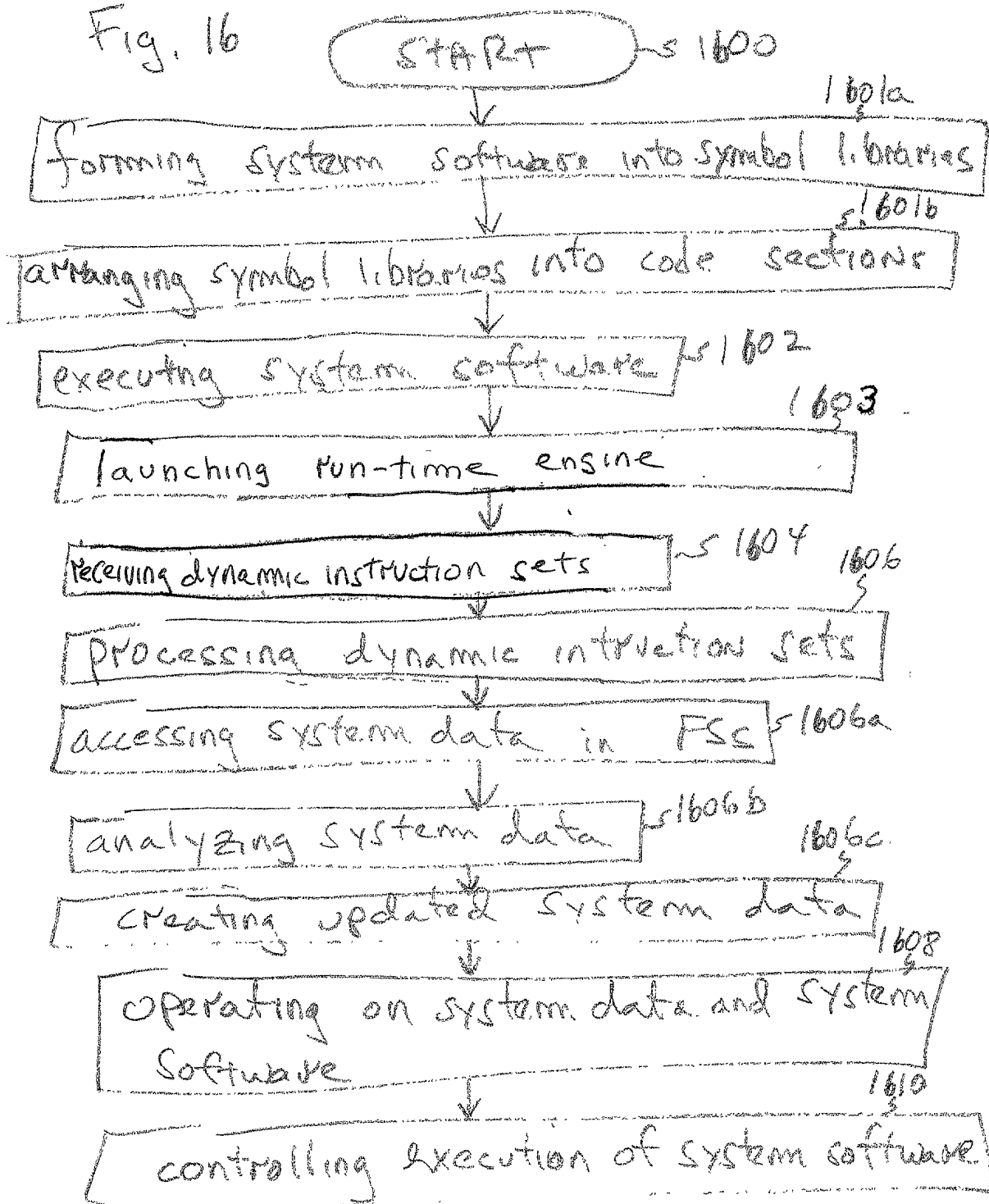


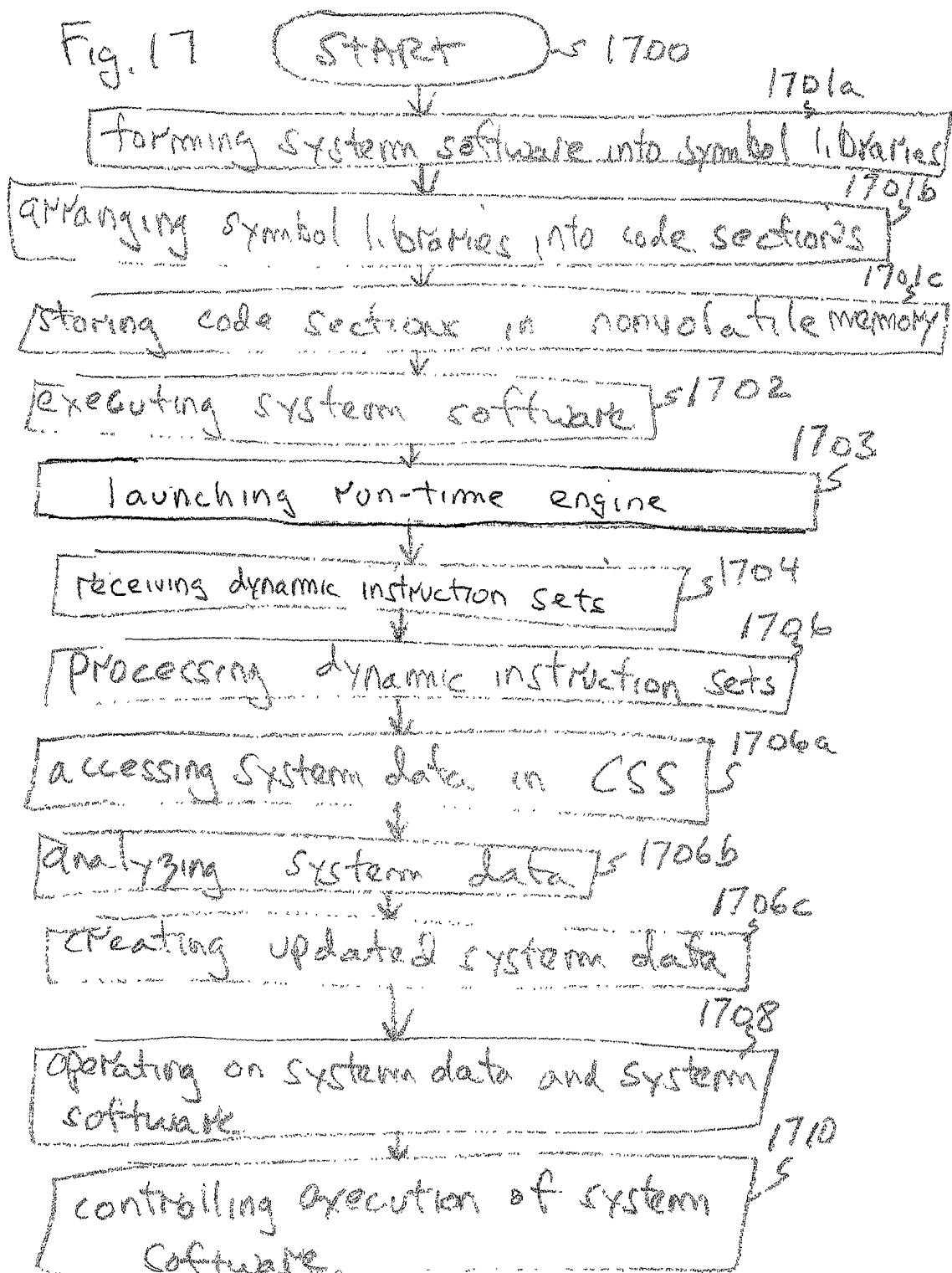
Fig. 156

Fig. 16



00070188 40004

Fig. 17



00070100 100004

Fig. 18

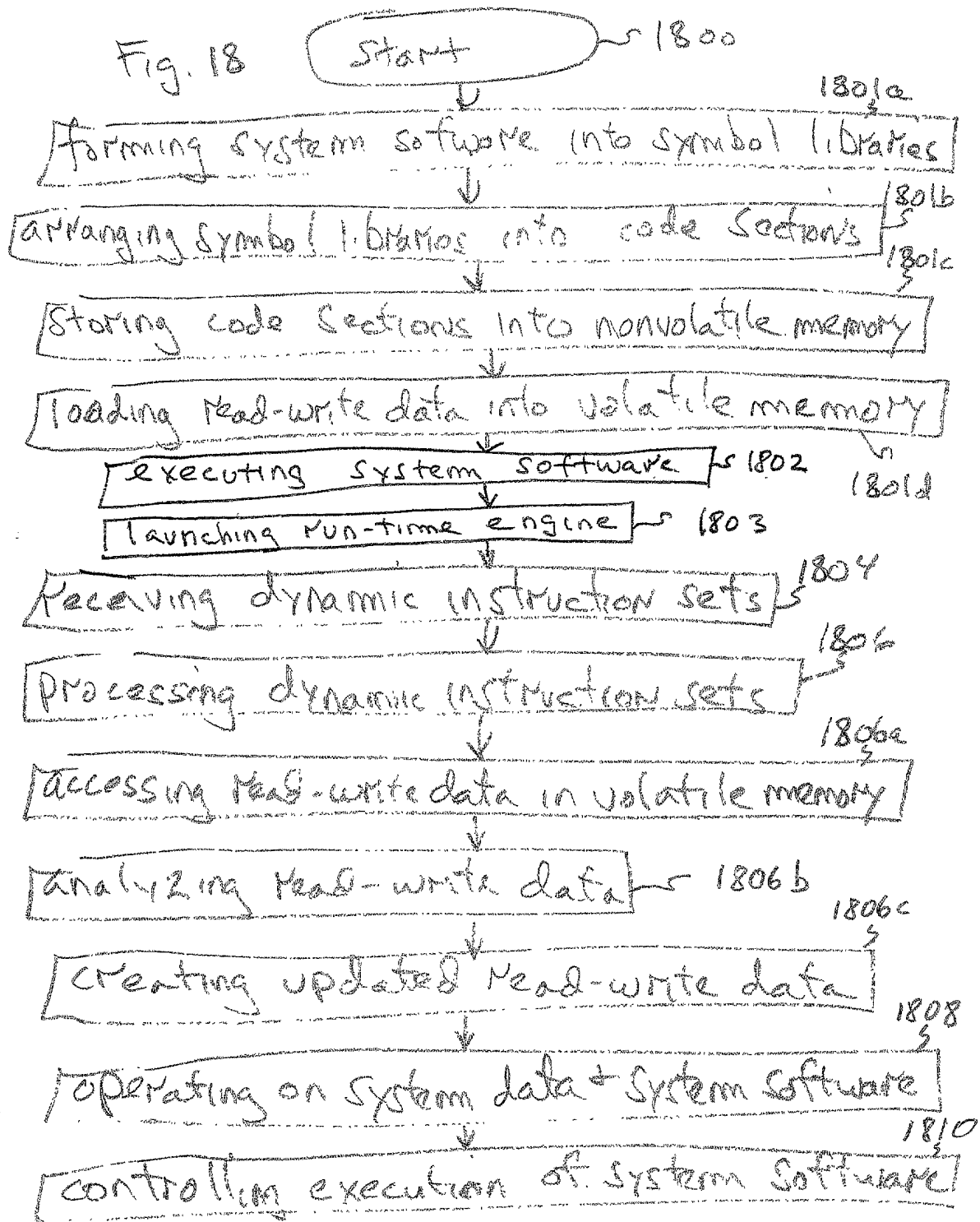
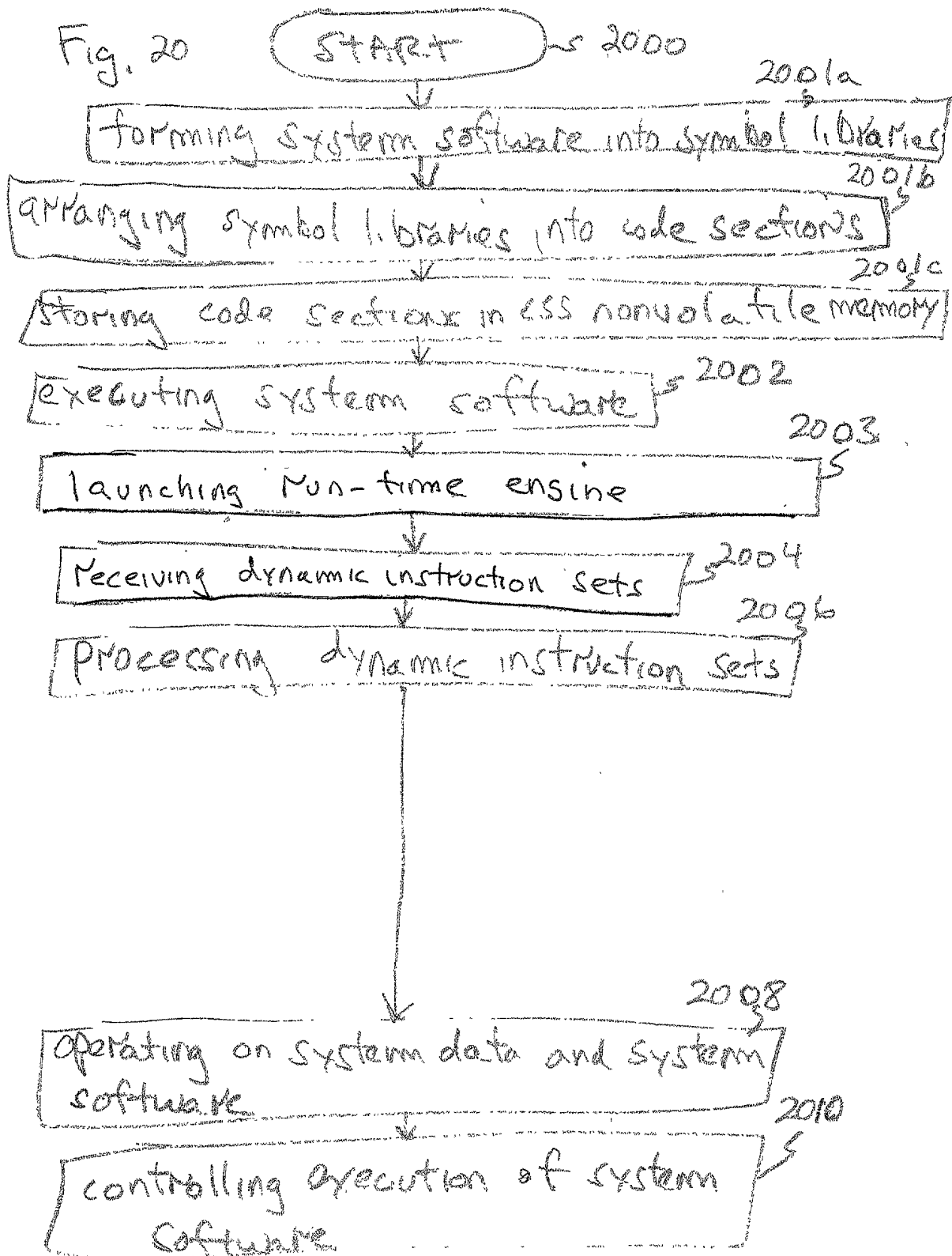


Fig. 20



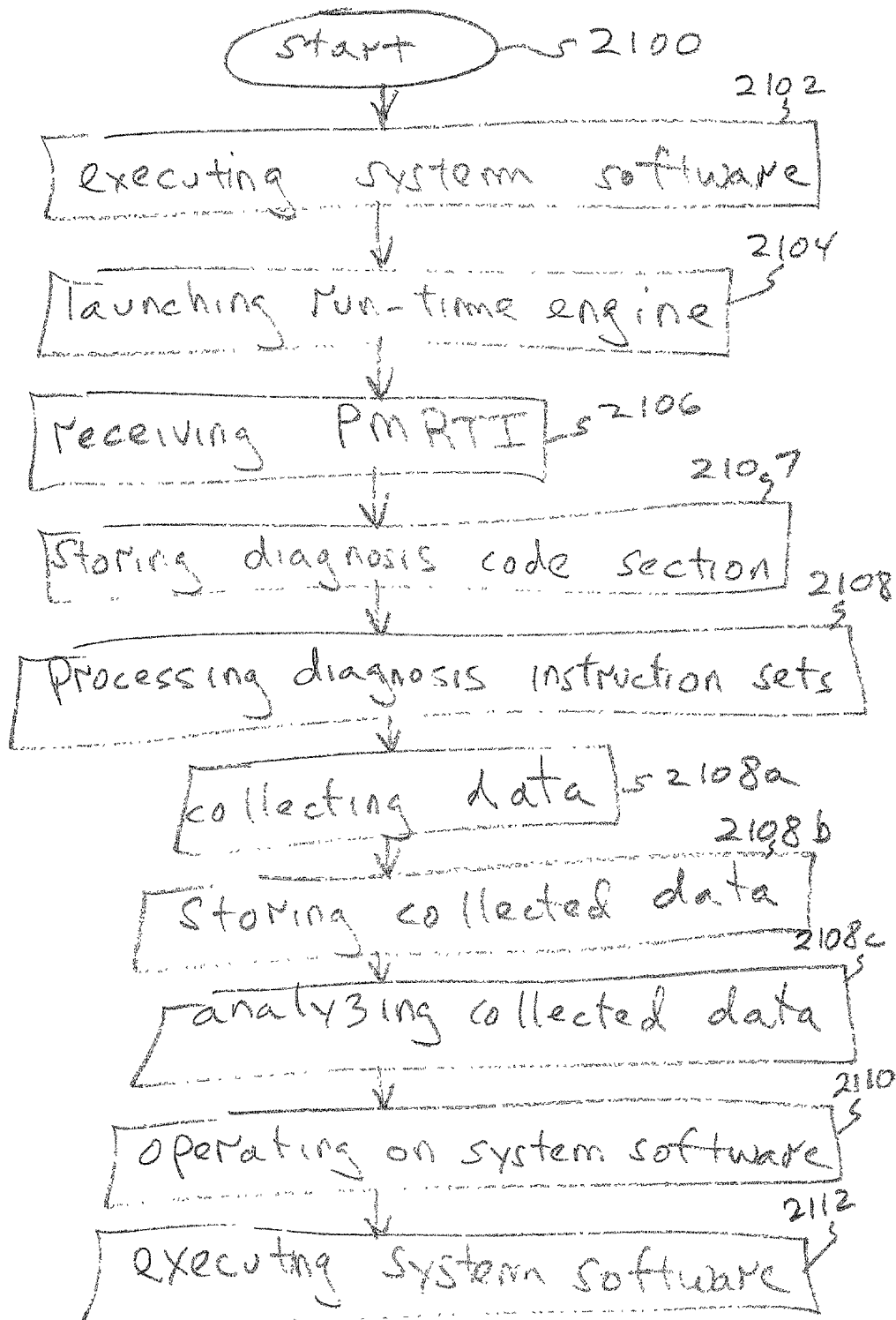
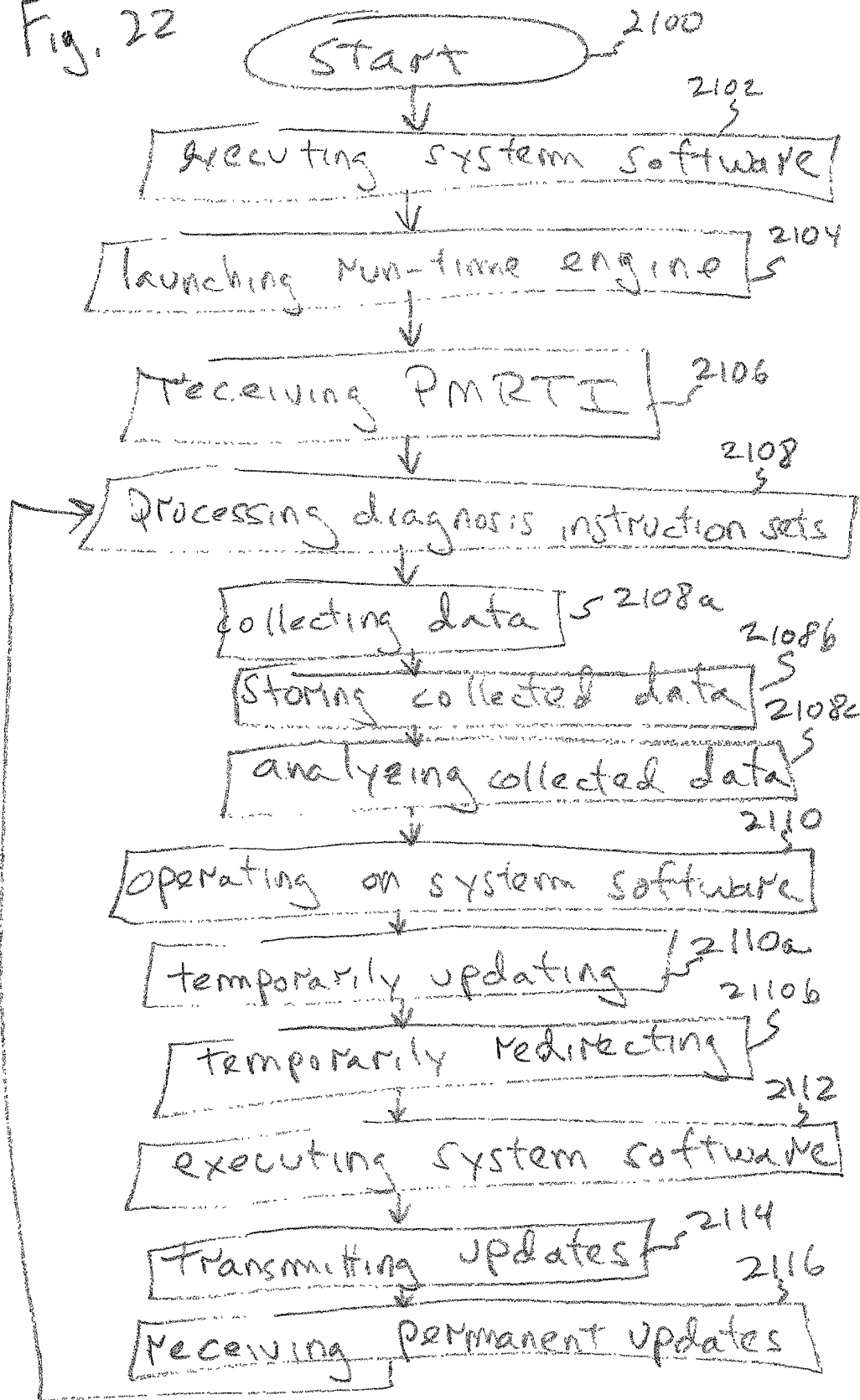


Fig. 21

Fig. 22



00970484 10094

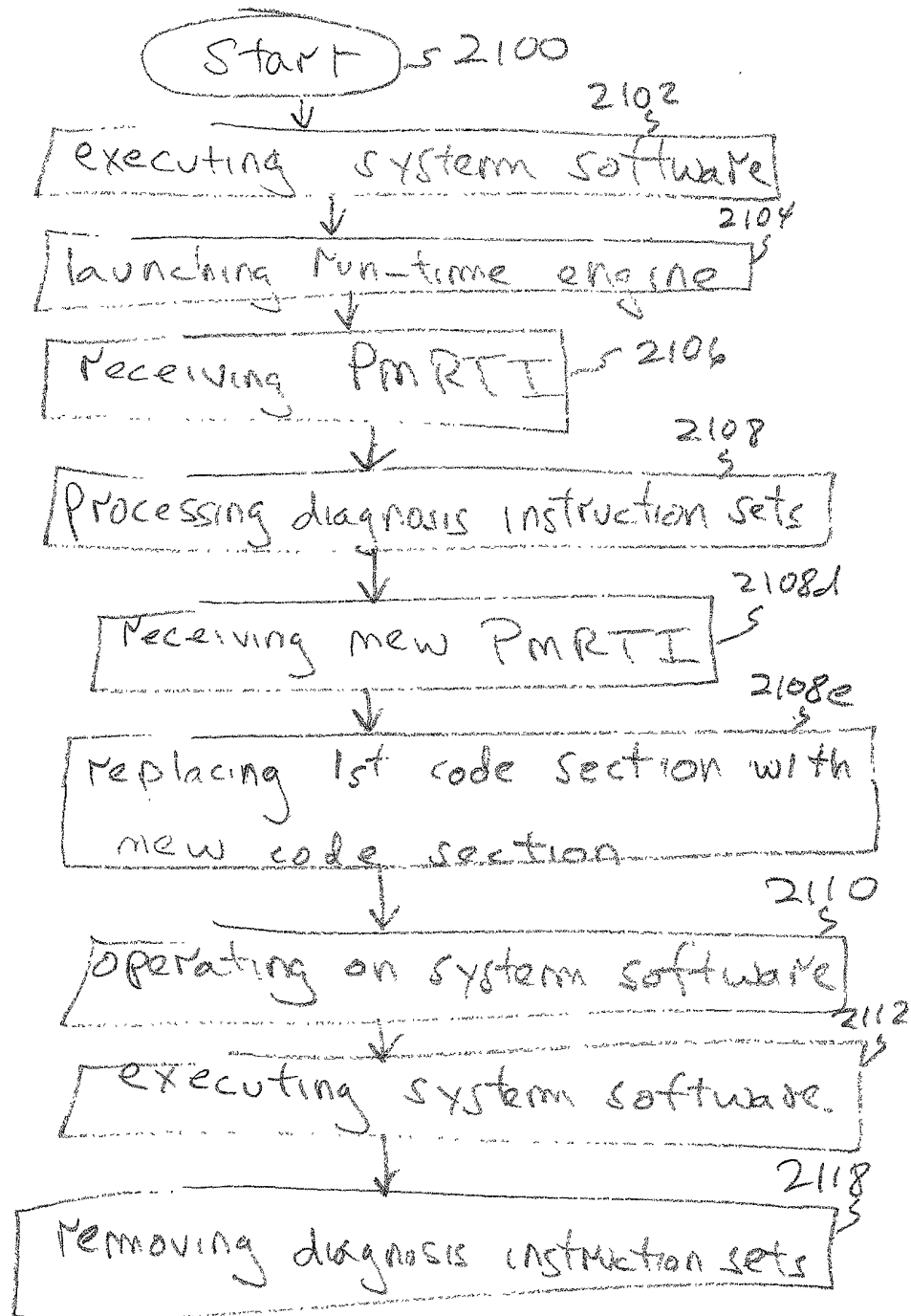


Fig. 23